FIG. 1

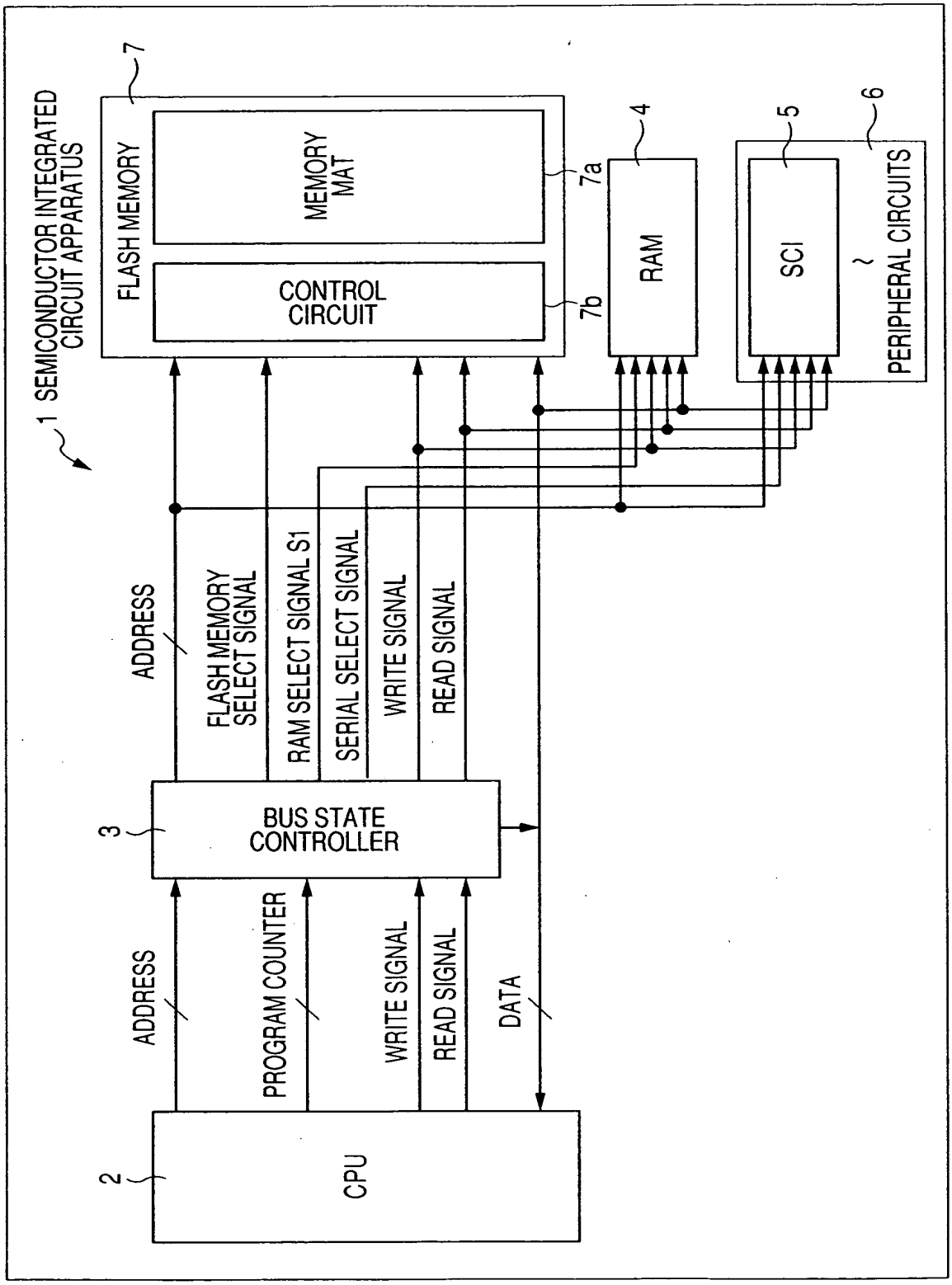

1 SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS
7
FLASH MEMORY
MEMORY MAT
7a
CONTROL CIRCUIT
7b
4
RAM
5
SCI
6
PERIPHERAL CIRCUITS
ADDRESS
FLASH MEMORY SELECT SIGNAL
RAM SELECT SIGNAL S1
SERIAL SELECT SIGNAL
WRITE SIGNAL
READ SIGNAL
3
BUS STATE CONTROLLER
ADDRESS
PROGRAM COUNTER
WRITE SIGNAL
READ SIGNAL
DATA
2
CPU

FIG. 2

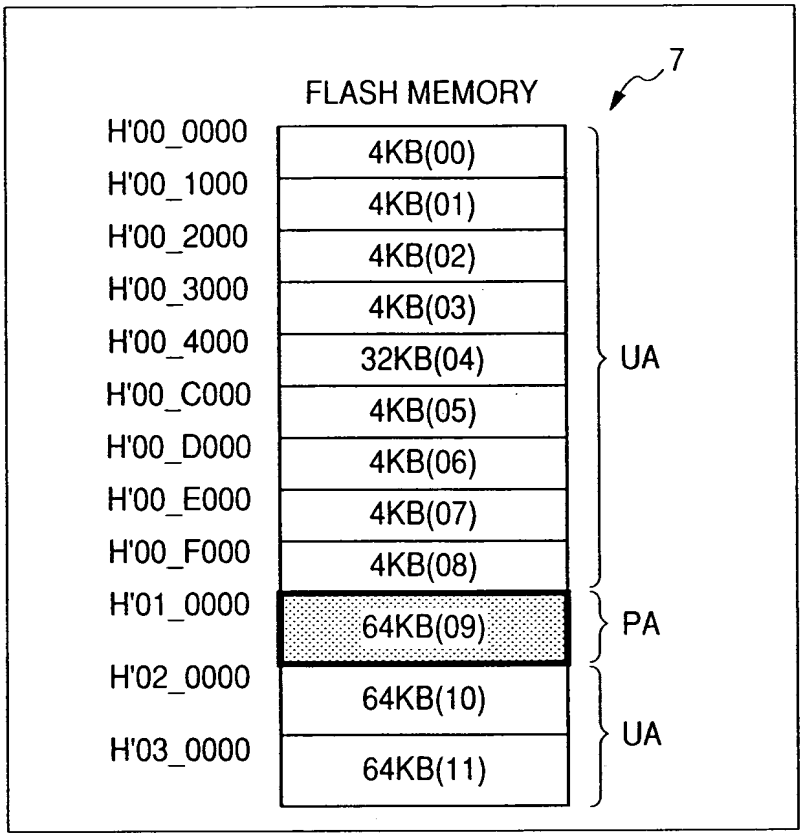

7
FLASH MEMORY
H'00_0000
H'00_1000
H'00_2000
H'00_3000
H'00_4000
H'00_C000
H'00_D000
H'00_E000
H'00_F000
H'01_0000
H'02_0000
H'03_0000
4KB(00)
4KB(01)
4KB(02)
4KB(03)
32KB(04)
4KB(05)
4KB(06)
4KB(07)
4KB(08)
64KB(09)
64KB(10)
64KB(11)
UA
PA
UA

FIG. 3

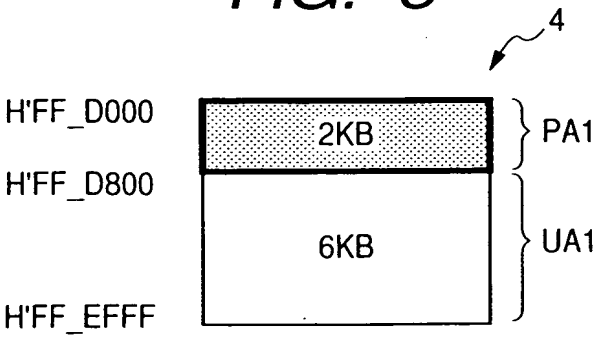

4
H'FF_D000
H'FF_D800
H'FF_EFFF
2KB
6KB
PA1
UA1

FIG. 4

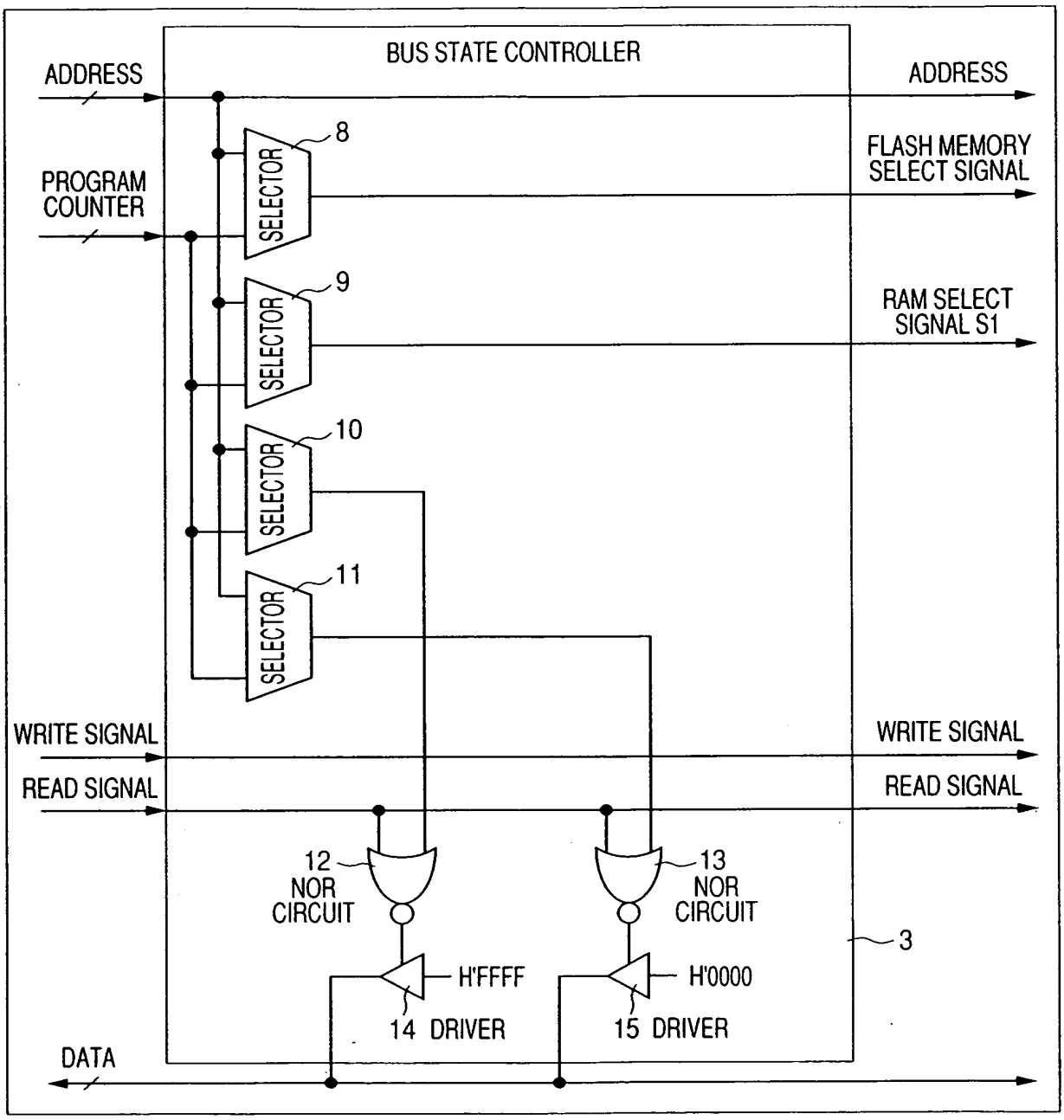

BUS STATE CONTROLLER
ADDRESS
ADDRESS
PROGRAM COUNTER
8
SELECTOR
FLASH MEMORY SELECT SIGNAL
9
SELECTOR
RAM SELECT SIGNAL S1
10
SELECTOR
11
SELECTOR
WRITE SIGNAL
WRITE SIGNAL
READ SIGNAL
READ SIGNAL
12
NOR CIRCUIT
13
NOR CIRCUIT
3
H'FFFF
H'0000
14 DRIVER
15 DRIVER
DATA

FIG. 5

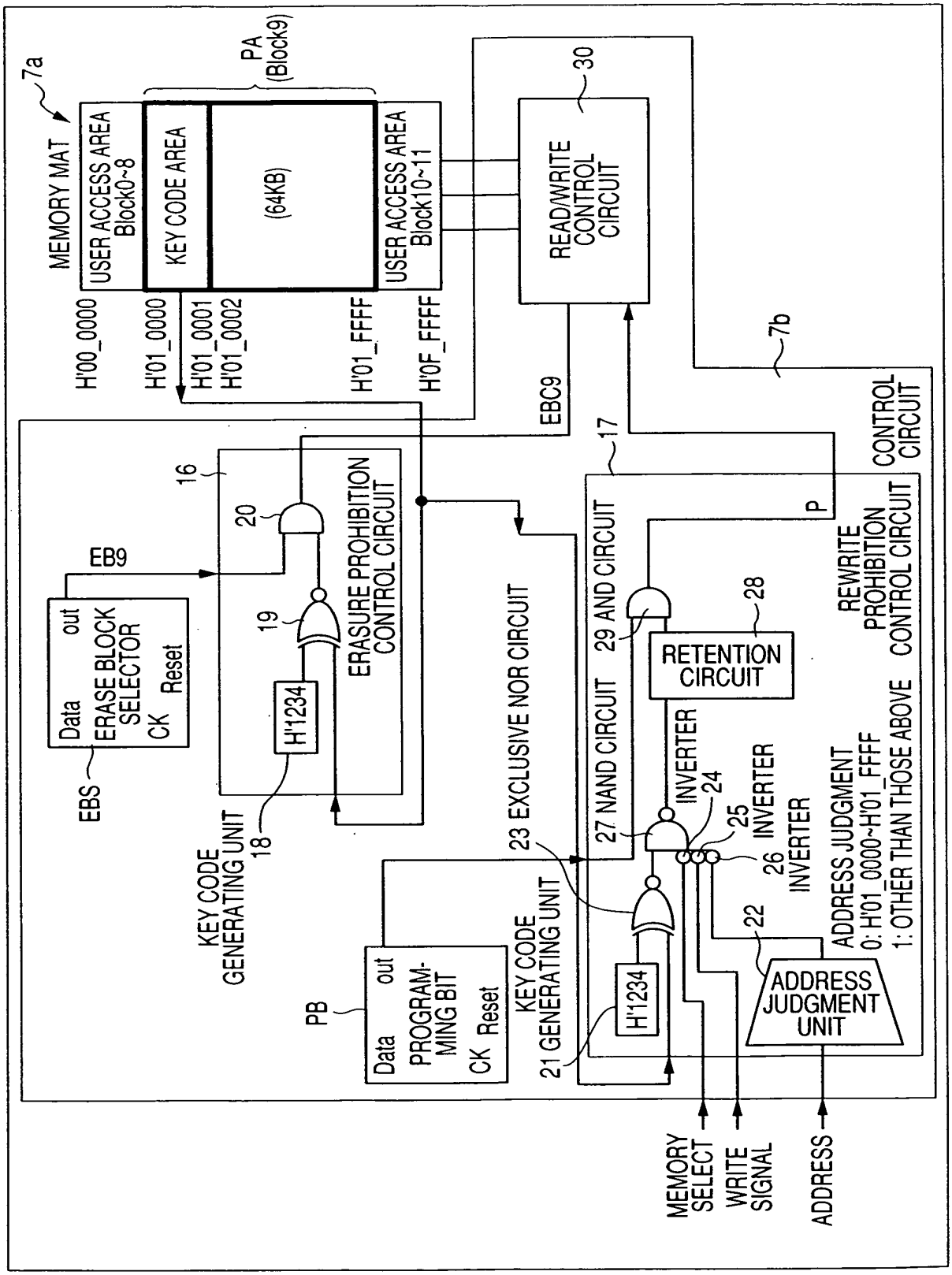

7a
MEMORY MAT
USER ACCESS AREA Block0~8
KEY CODE AREA
(64KB)
PA (Block9)
USER ACCESS AREA Block10~11
H'00_0000
H'01_0000
H'01_0001
H'01_0002
H'01_FFFF
H'0F_FFFF
READ/WRITE CONTROL CIRCUIT
30
EBC9
7b
CONTROL CIRCUIT
17
16
20
EB9
Data out
ERASE BLOCK SELECTOR
CK Reset
EBS
19
H'1234
ERASURE PROHIBITION CONTROL CIRCUIT
KEY CODE GENERATING UNIT
18
23 EXCLUSIVE NOR CIRCUIT
27 NAND CIRCUIT
29 AND CIRCUIT
P
28
RETENTION CIRCUIT
REWRITE PROHIBITION CONTROL CIRCUIT
INVERTER
24
25 INVERTER
26 INVERTER
ADDRESS JUDGMENT 0: H'01_0000~H'01_FFFF 1: OTHER THAN THOSE ABOVE
22
ADDRESS JUDGMENT UNIT
PB
Data out
PROGRAM-MING BIT
CK Reset
KEY CODE GENERATING UNIT
21
H'1234
MEMORY SELECT
WRITE SIGNAL
ADDRESS

FIG. 6

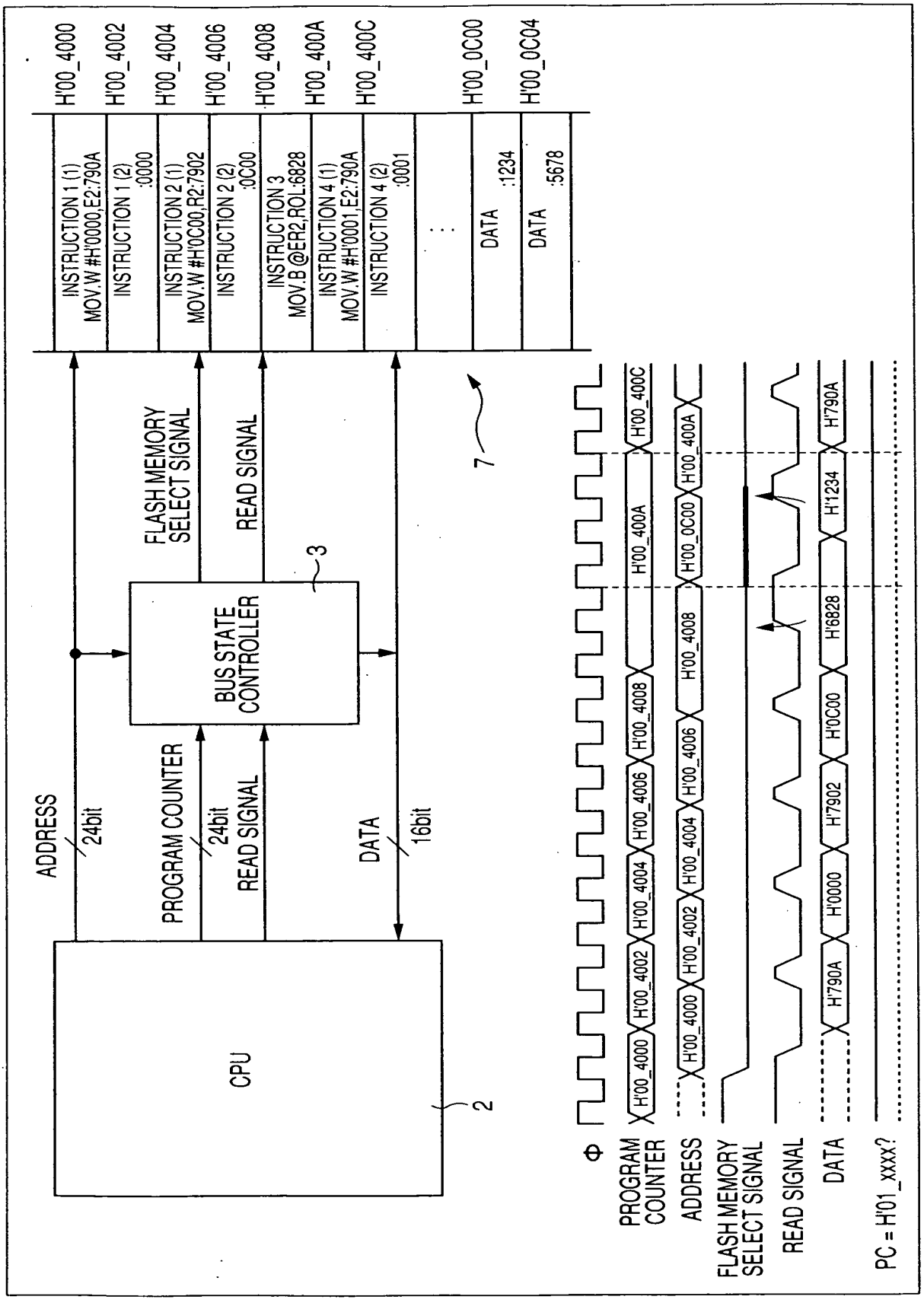

CPU
2
BUS STATE CONTROLLER
3
ADDRESS
24bit
PROGRAM COUNTER
24bit
READ SIGNAL
DATA
16bit
FLASH MEMORY SELECT SIGNAL
READ SIGNAL
7
H'00_4000 INSTRUCTION 1 (1) MOV.W #H'0000,E2:790A
H'00_4002 INSTRUCTION 1 (2) :0000
H'00_4004 INSTRUCTION 2 (1) MOV.W #H'0C00,R2:7902
H'00_4006 INSTRUCTION 2 (2) :0C00
H'00_4008 INSTRUCTION 3 MOV.B @ER2,ROL:6828
H'00_400A INSTRUCTION 4 (1) MOV.W #H'0001,E2:790A
H'00_400C INSTRUCTION 4 (2) :0001
H'00_0C00 DATA :1234
H'00_0C04 DATA :5678
Φ
PROGRAM COUNTER
ADDRESS
FLASH MEMORY SELECT SIGNAL
READ SIGNAL
DATA
PC = H'01_xxxx?
H'00_4000
H'00_4002
H'00_4004
H'00_4006
H'00_4008
H'00_400A
H'00_400C
H'00_0C00
H'790A
H'0000
H'7902
H'0C00
H'6828
H'1234
H'790A

FIG. 7

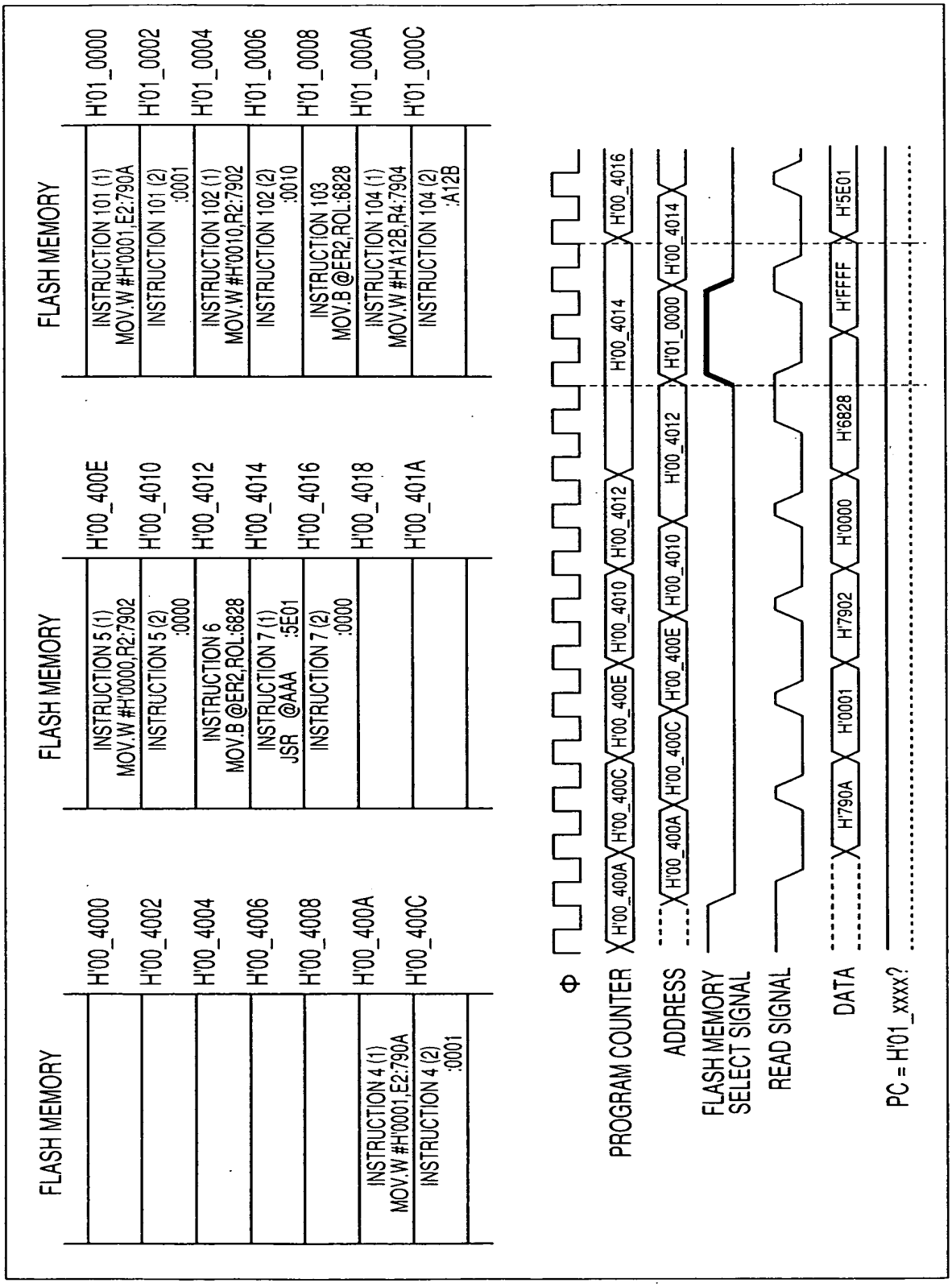

FLASH MEMORY
H'00_4000
H'00_4002
H'00_4004
H'00_4006
H'00_4008
H'00_400A
H'00_400C
INSTRUCTION 4 (1)
MOV.W #H'0001,E2:790A
INSTRUCTION 4 (2)
:0001
FLASH MEMORY
H'00_400E
H'00_4010
H'00_4012
H'00_4014
H'00_4016
H'00_4018
H'00_401A
INSTRUCTION 5 (1)
MOV.W #H'0000,R2:7902
INSTRUCTION 5 (2)
:0000
INSTRUCTION 6
MOV.B @ER2,ROL:6828
INSTRUCTION 7 (1)
JSR @AAA :5E01
INSTRUCTION 7 (2)
:0000
FLASH MEMORY
H'01_0000
H'01_0002
H'01_0004
H'01_0006
H'01_0008
H'01_000A
H'01_000C
INSTRUCTION 101 (1)
MOV.W #H'0001,E2:790A
INSTRUCTION 101 (2)
:0001
INSTRUCTION 102 (1)
MOV.W #H'0010,R2:7902
INSTRUCTION 102 (2)
:0010
INSTRUCTION 103
MOV.B @ER2,ROL:6828
INSTRUCTION 104 (1)
MOV.W #H'A12B,R4:7904
INSTRUCTION 104 (2)
:A12B
Φ
PROGRAM COUNTER
H'00_400A
H'00_400C
H'00_400E
H'00_4010
H'00_4012
H'00_4014
H'00_4016
ADDRESS
H'00_400A
H'00_400C
H'00_400E
H'00_4010
H'00_4012
H'01_0000
H'00_4014
FLASH MEMORY SELECT SIGNAL
READ SIGNAL
DATA
H'790A
H'0001
H'7902
H'0000
H'6828
H'FFFF
H'5E01
PC = H'01_xxxx?

FIG. 8

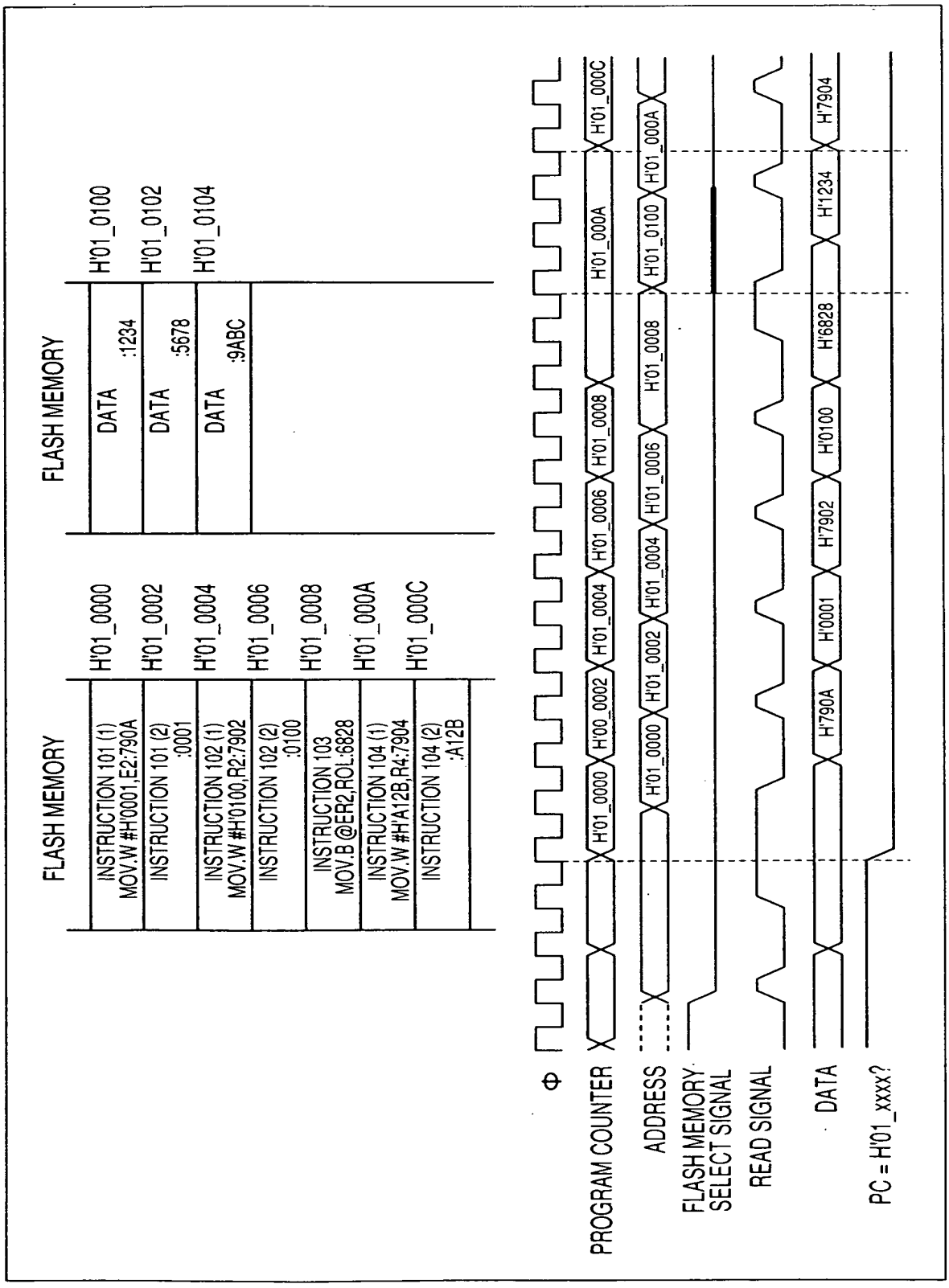

FLASH MEMORY
H'01_0000
INSTRUCTION 101 (1)
MOV.W #H'0001,E2:790A
H'01_0002
INSTRUCTION 101 (2)
:0001
H'01_0004
INSTRUCTION 102 (1)
MOV.W #H'0100,R2:7902
H'01_0006
INSTRUCTION 102 (2)
:0100
H'01_0008
INSTRUCTION 103
MOV.B @ER2,ROL:6828
H'01_000A
INSTRUCTION 104 (1)
MOV.W #H'A12B,R4:7904
H'01_000C
INSTRUCTION 104 (2)
:A12B
FLASH MEMORY
H'01_0100
DATA :1234
H'01_0102
DATA :5678
H'01_0104
DATA :9ABC
Φ
PROGRAM COUNTER
H'01_0000
H'00_0002
H'01_0004
H'01_0006
H'01_0008
H'01_000A
H'01_000C
ADDRESS
H'01_0000
H'01_0002
H'01_0004
H'01_0006
H'01_0008
H'01_0100
H'01_000A
FLASH MEMORY SELECT SIGNAL
READ SIGNAL
DATA
H'790A
H'0001
H'7902
H'0100
H'6828
H'1234
H'7904
PC = H'01_xxxx?

FIG. 9

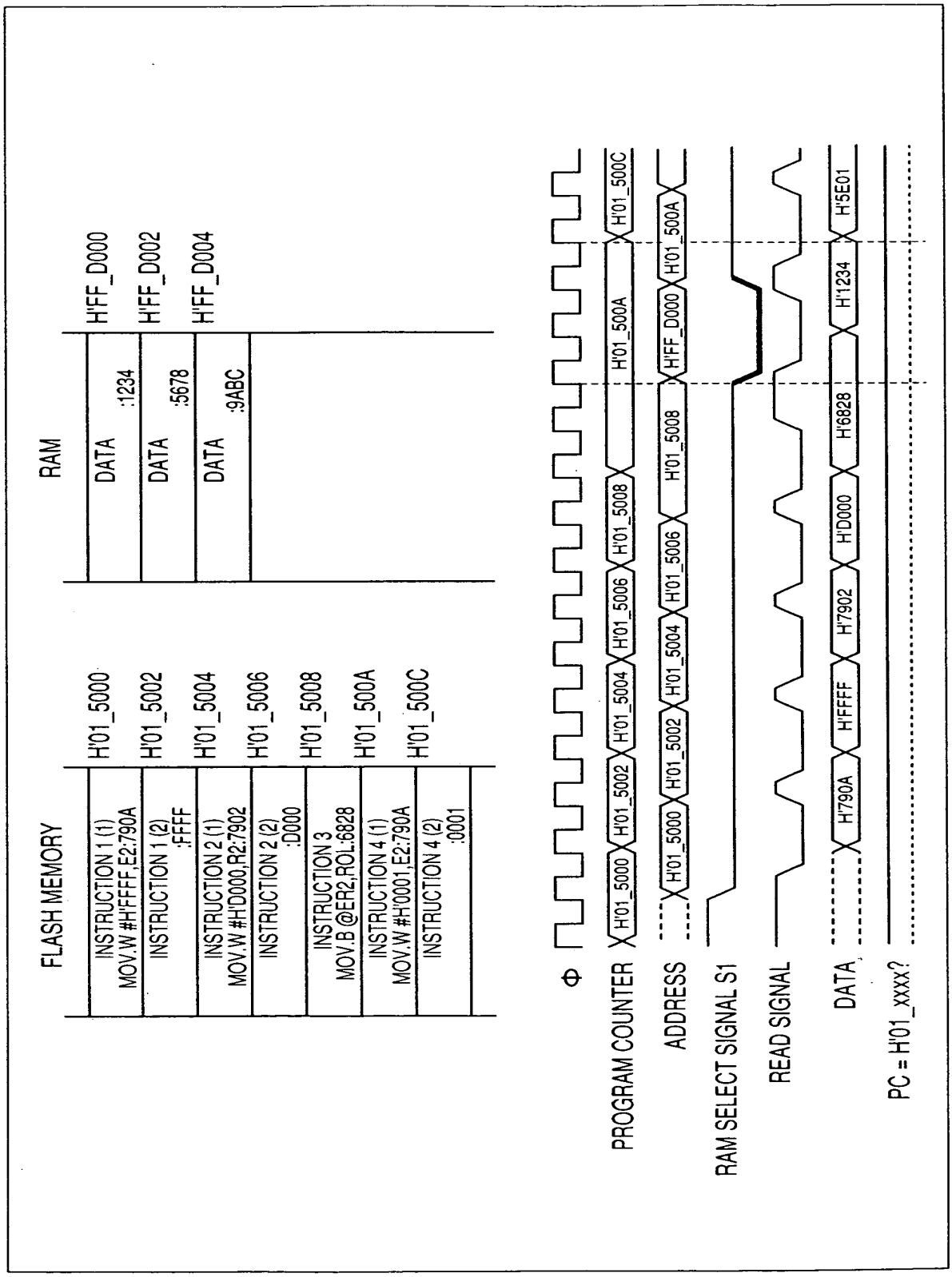

FLASH MEMORY
H'01_5000
INSTRUCTION 1 (1)
MOV.W #H'FFFF,E2:790A
H'01_5002
INSTRUCTION 1 (2)
:FFFF
H'01_5004
INSTRUCTION 2 (1)
MOV.W #H'D000,R2:7902
H'01_5006
INSTRUCTION 2 (2)
:D000
H'01_5008
INSTRUCTION 3
MOV.B @ER2,ROL:6828
H'01_500A
INSTRUCTION 4 (1)
MOV.W #H'0001,E2:790A
H'01_500C
INSTRUCTION 4 (2)
:0001
RAM
H'FF_D000
DATA :1234
H'FF_D002
DATA :5678
H'FF_D004
DATA :9ABC
Φ
PROGRAM COUNTER
ADDRESS
RAM SELECT SIGNAL S1
READ SIGNAL
DATA
PC = H'01_xxxx?
H'01_5000
H'01_5002
H'01_5004
H'01_5006
H'01_5008
H'01_500A
H'01_500C
H'790A
H'FFFF
H'7902
H'D000
H'6828
H'1234
H'5E01

FIG. 10

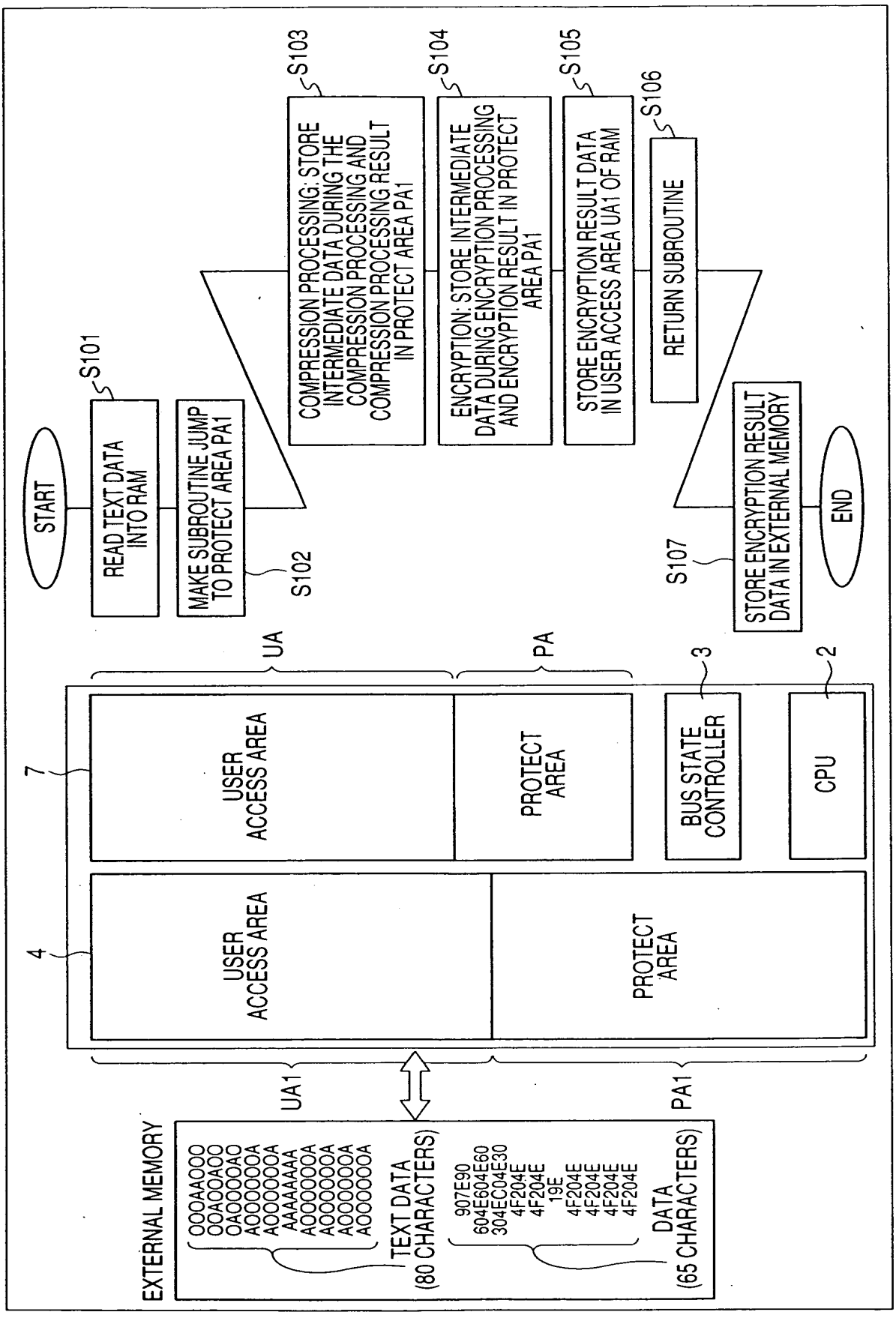

START
S101
READ TEXT DATA INTO RAM
MAKE SUBROUTINE JUMP TO PROTECT AREA PA1
S102
S103
COMPRESSION PROCESSING: STORE INTERMEDIATE DATA DURING THE COMPRESSION PROCESSING AND COMPRESSION PROCESSING RESULT IN PROTECT AREA PA1
S104
ENCRYPTION: STORE INTERMEDIATE DATA DURING ENCRYPTION PROCESSING AND ENCRYPTION RESULT IN PROTECT AREA PA1
S105
STORE ENCRYPTION RESULT DATA IN USER ACCESS AREA UA1 OF RAM
S106
RETURN SUBROUTINE
S107
STORE ENCRYPTION RESULT DATA IN EXTERNAL MEMORY
END
UA
PA
7
USER ACCESS AREA
PROTECT AREA
3
BUS STATE CONTROLLER
2
CPU
4
USER ACCESS AREA
PROTECT AREA
UA1
PA1
EXTERNAL MEMORY
TEXT DATA (80 CHARACTERS)
OOOAAOOO
OOAOOAOO
OAOOOOAO
AOOOOOOA
AOOOOOOA
AAAAAAAA
AOOOOOOA
AOOOOOOA
AOOOOOOA
AOOOOOOA
DATA (65 CHARACTERS)
907E90
604E604E60
304EC04E30
4F204E
4F204E
19E
4F204E
4F204E
4F204E
4F204E

FIG. 11

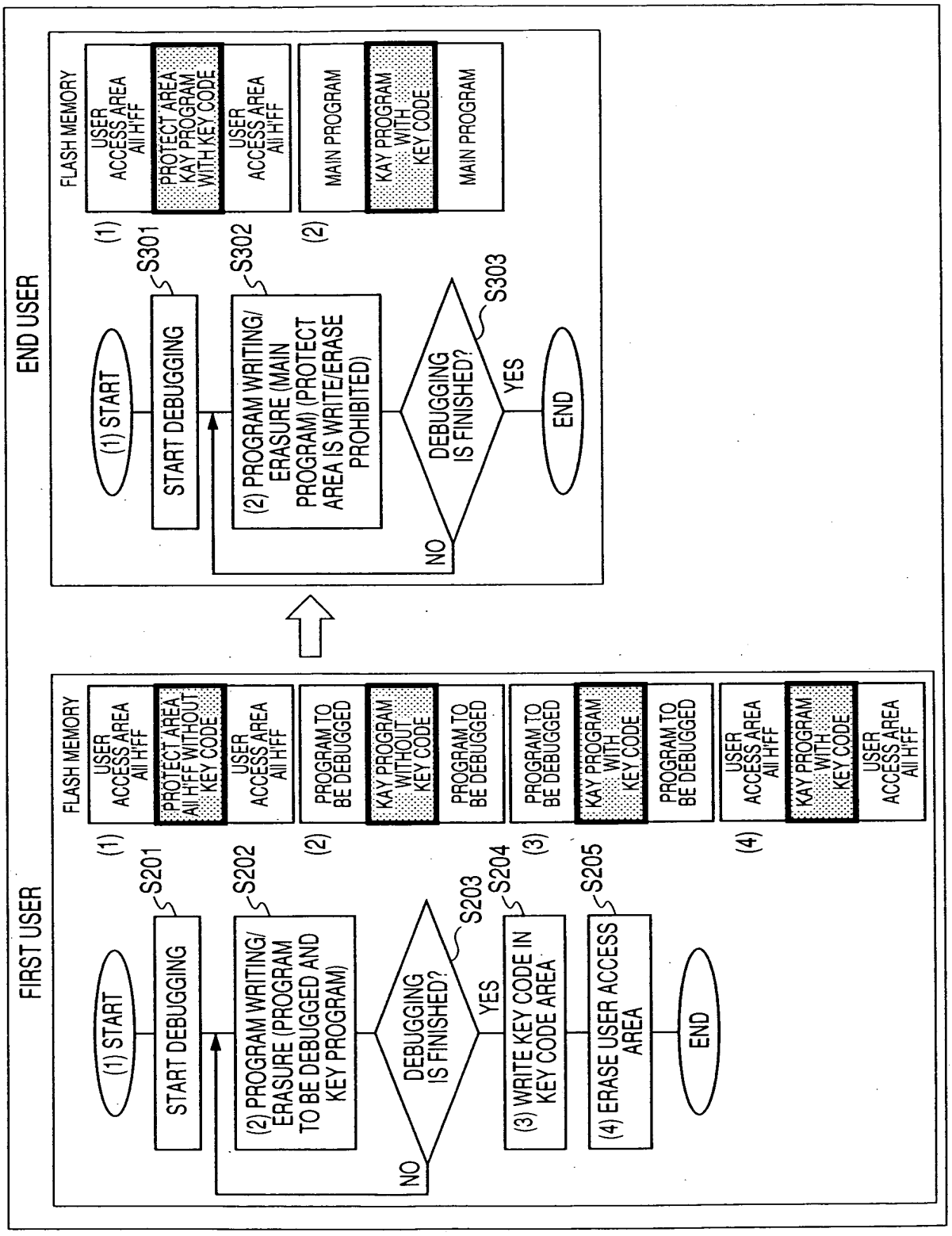

FIRST USER
END USER
FLASH MEMORY
USER ACCESS AREA All H'FF
PROTECT AREA All H'FF WITHOUT KEY CODE
USER ACCESS AREA All H'FF
PROGRAM TO BE DEBUGGED
KAY PROGRAM WITHOUT KEY CODE
PROGRAM TO BE DEBUGGED
PROGRAM TO BE DEBUGGED
KAY PROGRAM WITH KEY CODE
PROGRAM TO BE DEBUGGED
USER ACCESS AREA All H'FF
KAY PROGRAM WITH KEY CODE
USER ACCESS AREA All H'FF
(1)
(2)
(3)
(4)
(1) START
START DEBUGGING
(2) PROGRAM WRITING/ ERASURE (PROGRAM TO BE DEBUGGED AND KEY PROGRAM)
DEBUGGING IS FINISHED?
NO
YES
(3) WRITE KEY CODE IN KEY CODE AREA
(4) ERASE USER ACCESS AREA
END
S201
S202
S203
S204
S205
FLASH MEMORY
USER ACCESS AREA All H'FF
PROTECT AREA KAY PROGRAM WITH KEY CODE
USER ACCESS AREA All H'FF
MAIN PROGRAM
KAY PROGRAM WITH KEY CODE
MAIN PROGRAM
(1)
(2)
(1) START
START DEBUGGING
(2) PROGRAM WRITING/ ERASURE (MAIN PROGRAM) (PROTECT AREA IS WRITE/ERASE PROHIBITED)
DEBUGGING IS FINISHED?
NO
YES
END
S301
S302
S303

FIG. 12

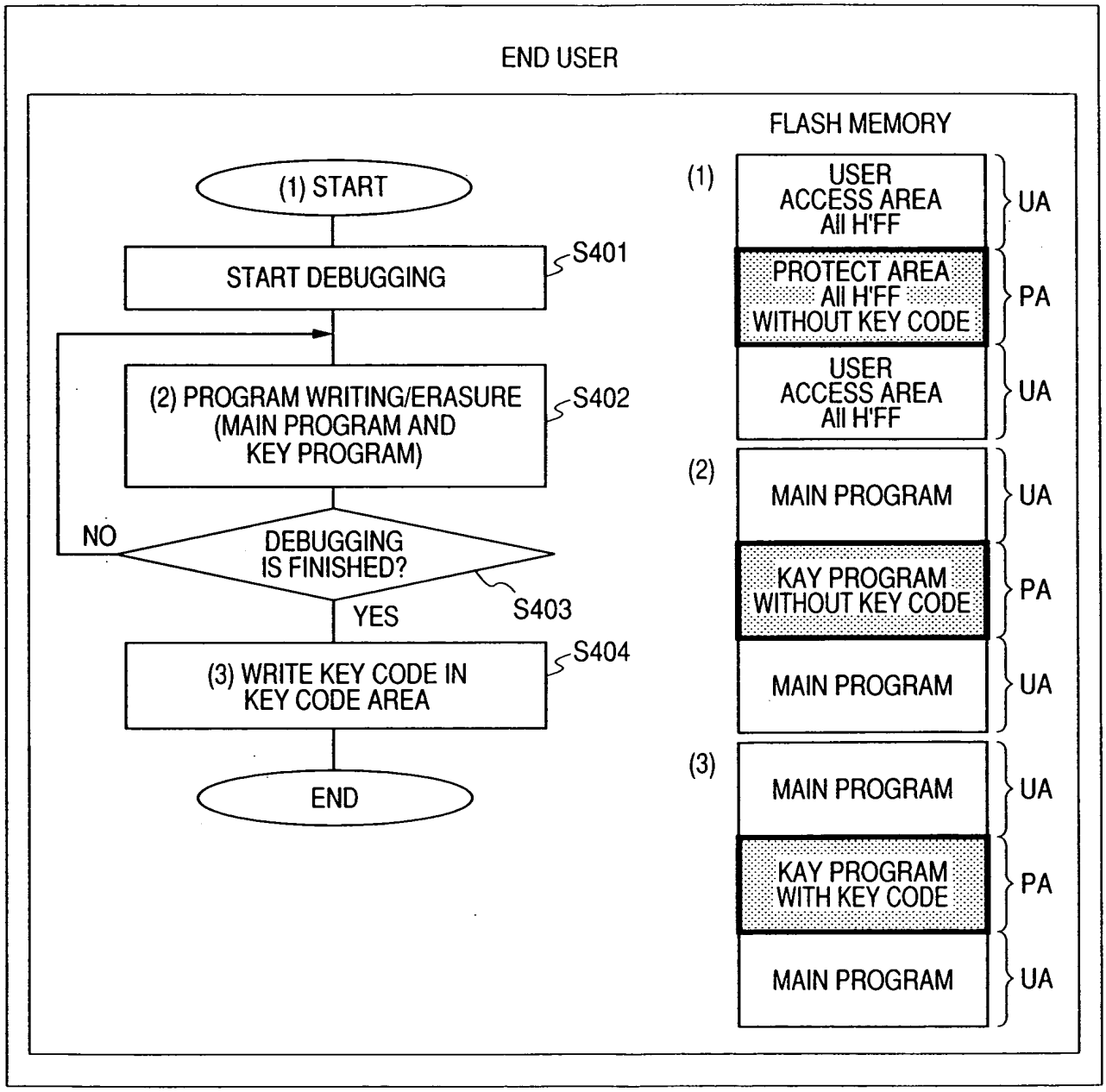

END USER
(1) START
START DEBUGGING
S401
(2) PROGRAM WRITING/ERASURE (MAIN PROGRAM AND KEY PROGRAM)
S402
NO
DEBUGGING IS FINISHED?
S403
YES
(3) WRITE KEY CODE IN KEY CODE AREA
S404
END
FLASH MEMORY
(1)
USER ACCESS AREA All H'FF
UA
PROTECT AREA All H'FF WITHOUT KEY CODE
PA
USER ACCESS AREA All H'FF
UA
(2)
MAIN PROGRAM
UA
KAY PROGRAM WITHOUT KEY CODE
PA
MAIN PROGRAM
UA
(3)
MAIN PROGRAM
UA
KAY PROGRAM WITH KEY CODE
PA
MAIN PROGRAM
UA

FIG. 13

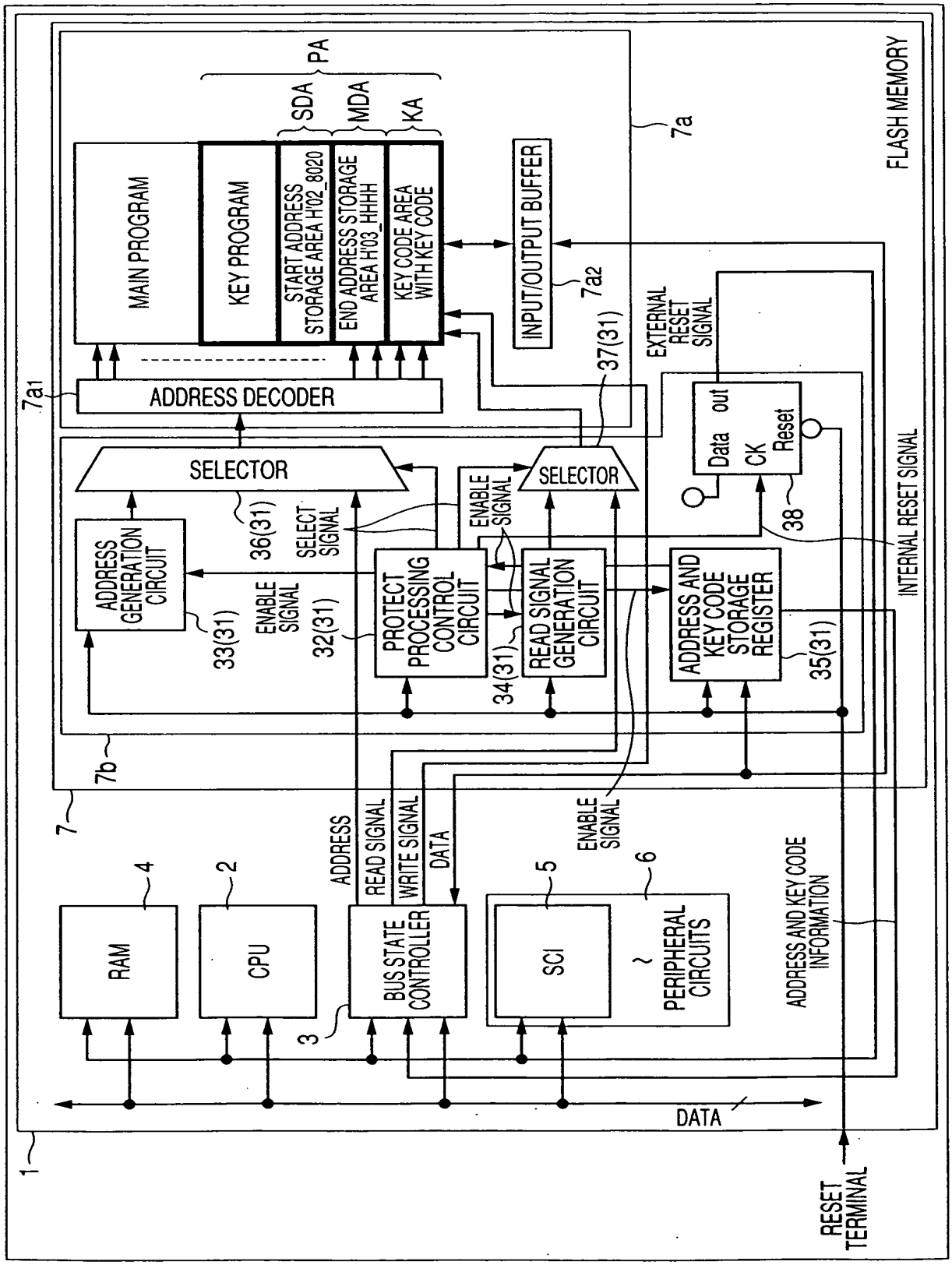

FLASH MEMORY
PA
SDA
MDA
KA
MAIN PROGRAM
KEY PROGRAM
START ADDRESS STORAGE AREA H'02_8020
END ADDRESS STORAGE AREA H'03_HHHH
KEY CODE AREA WITH KEY CODE
7a
INPUT/OUTPUT BUFFER
7a2
37(31)
EXTERNAL RESET SIGNAL
7a1
ADDRESS DECODER
SELECTOR
36(31)
SELECT SIGNAL
ENABLE SIGNAL
SELECTOR
Data out
CK
Reset
38
INTERNAL RESET SIGNAL
ADDRESS GENERATION CIRCUIT
33(31)
ENABLE SIGNAL
32(31)
PROTECT PROCESSING CONTROL CIRCUIT
34(31)
READ SIGNAL GENERATION CIRCUIT
ADDRESS AND KEY CODE STORAGE REGISTER
35(31)
7b
7
ADDRESS
READ SIGNAL
WRITE SIGNAL
DATA
ENABLE SIGNAL
4
2
5
6
RAM
CPU
BUS STATE CONTROLLER
SCI
PERIPHERAL CIRCUITS
ADDRESS AND KEY CODE INFORMATION
3
DATA
1
RESET TERMINAL

FIG. 14

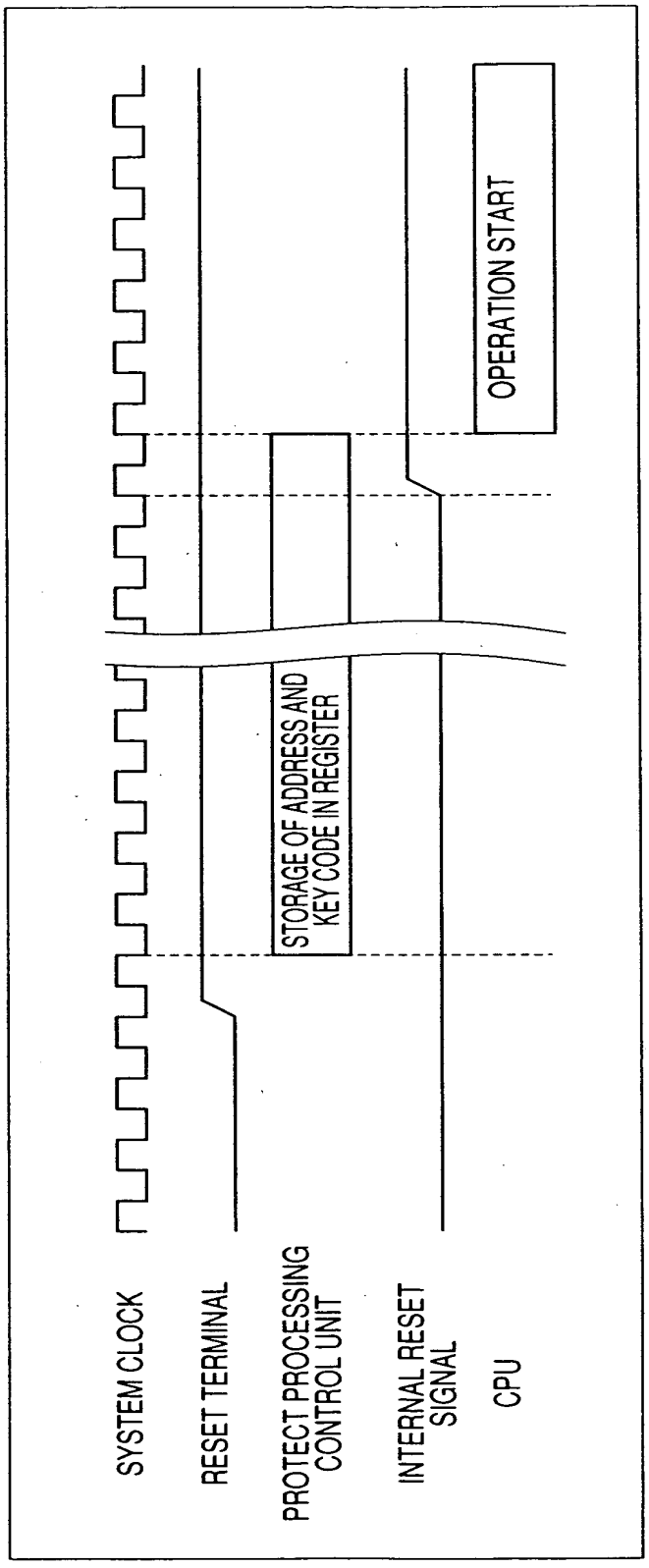

SYSTEM CLOCK
RESET TERMINAL
PROTECT PROCESSING CONTROL UNIT
INTERNAL RESET SIGNAL
CPU
STORAGE OF ADDRESS AND KEY CODE IN REGISTER
OPERATION START

FIG. 15

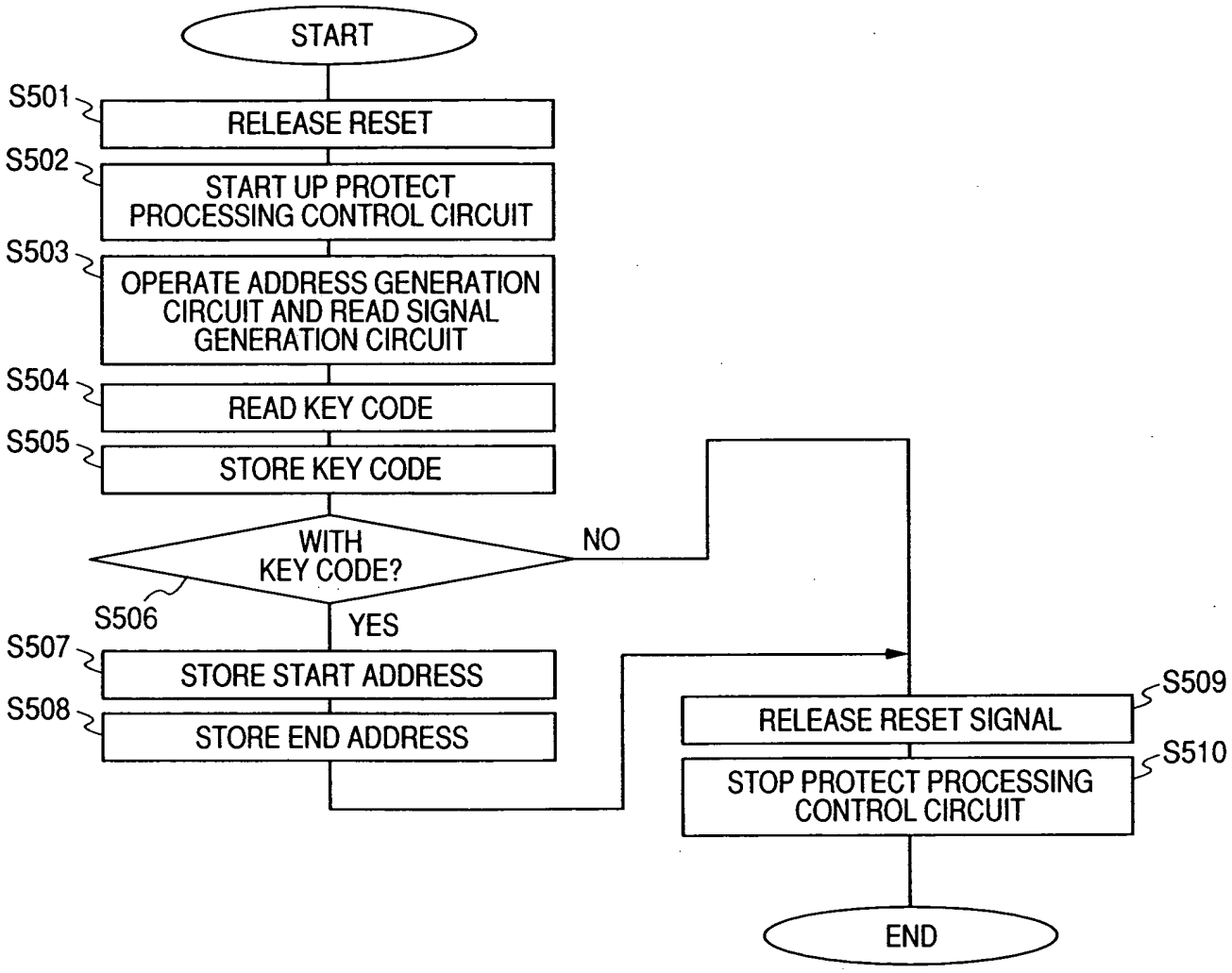

START
S501
RELEASE RESET
S502
START UP PROTECT PROCESSING CONTROL CIRCUIT
S503
OPERATE ADDRESS GENERATION CIRCUIT AND READ SIGNAL GENERATION CIRCUIT
S504
READ KEY CODE
S505
STORE KEY CODE
WITH KEY CODE?
S506
NO
YES
S507
STORE START ADDRESS
S508
STORE END ADDRESS
S509
RELEASE RESET SIGNAL
S510
STOP PROTECT PROCESSING CONTROL CIRCUIT
END

FIG. 16

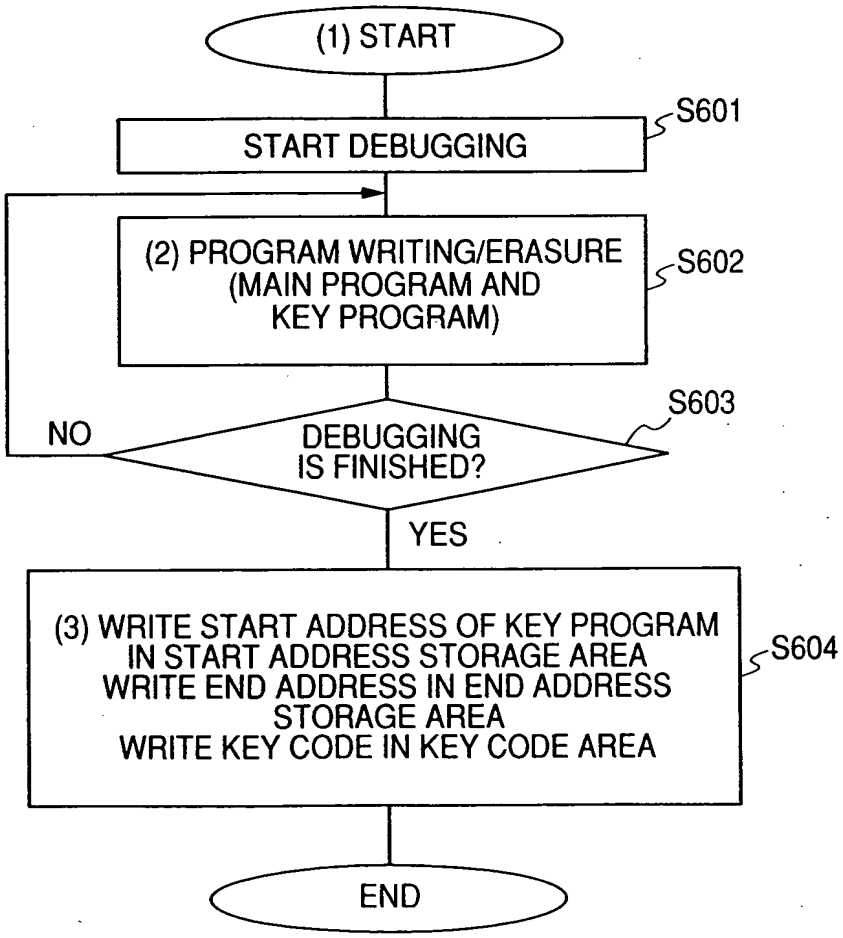
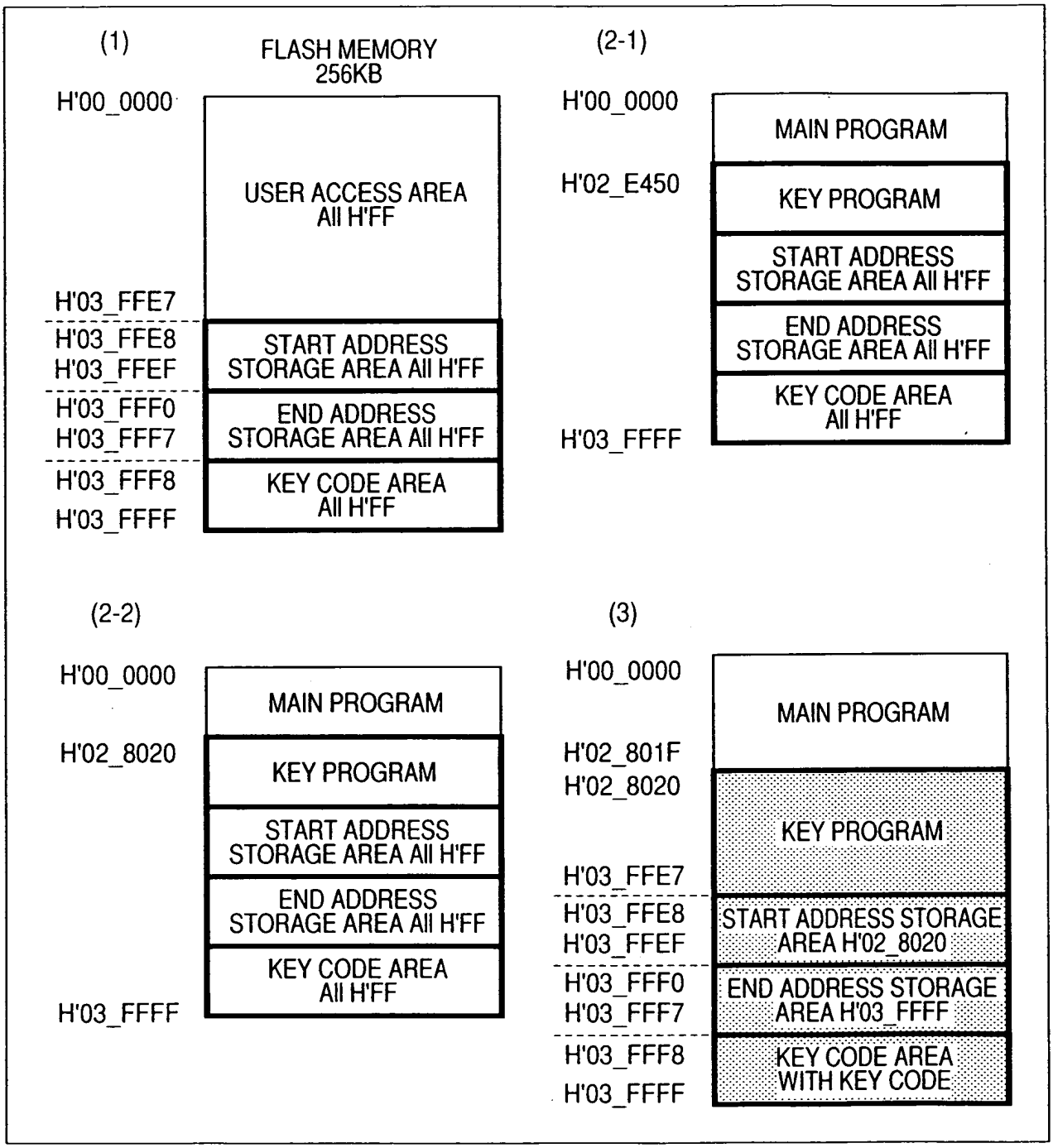

(1) START
START DEBUGGING
S601
(2) PROGRAM WRITING/ERASURE
(MAIN PROGRAM AND
KEY PROGRAM)
S602
S603
NO
DEBUGGING
IS FINISHED?
YES
(3) WRITE START ADDRESS OF KEY PROGRAM
IN START ADDRESS STORAGE AREA
WRITE END ADDRESS IN END ADDRESS
STORAGE AREA
WRITE KEY CODE IN KEY CODE AREA
S604
END

FIG. 17


(1)
FLASH MEMORY
256KB
H'00_0000
USER ACCESS AREA
All H'FF
H'03_FFE7
H'03_FFE8
H'03_FFEF
START ADDRESS
STORAGE AREA All H'FF
H'03_FFF0
H'03_FFF7
END ADDRESS
STORAGE AREA All H'FF
H'03_FFF8
H'03_FFFF
KEY CODE AREA
All H'FF
(2-1)
H'00_0000
MAIN PROGRAM
H'02_E450
KEY PROGRAM
START ADDRESS
STORAGE AREA All H'FF
END ADDRESS
STORAGE AREA All H'FF
KEY CODE AREA
All H'FF
H'03_FFFF
(2-2)
H'00_0000
MAIN PROGRAM
H'02_8020
KEY PROGRAM
START ADDRESS
STORAGE AREA All H'FF
END ADDRESS
STORAGE AREA All H'FF
KEY CODE AREA
All H'FF
H'03_FFFF
(3)
H'00_0000
MAIN PROGRAM
H'02_801F
H'02_8020
KEY PROGRAM
H'03_FFE7
H'03_FFE8
H'03_FFEF
START ADDRESS STORAGE
AREA H'02_8020
H'03_FFF0
H'03_FFF7
END ADDRESS STORAGE
AREA H'03_FFFF
H'03_FFF8
H'03_FFFF
KEY CODE AREA
WITH KEY CODE